Critical Chip-Level Examination on GAA Technology with Dual-sided Interconnects from BSPDN to Backside Clock: Architecture Innovations, PPA and First Signal/Power Integrity Analysis

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***Abstract* —This work thoroughly investigated the Gate-All-Around (GAA) transistors at 2nm node along with critical backside interconnect (BSI) evolutions. BSI was also experimentally demonstrated on a FinFET test vehicle. Beyond BS power delivery network (BSPDN), we also examined next-generation BSI technology: BS clock and the BS direct contact (BSC) process scheme. Enabled by all the clock network allocated to the BS, this BS-only clock architecture outperforms the conventional frontside (FS) PDN (FSPDN) by 26.9% in RO speed. At the chip level, for the first time, power integrity (PI), signal integrity (SI) and clock quality were analyzed on BS-only clock. BS clock network is inserted into the tight-meshed BSPDN that only leads to a mild bounce of IR drop from 5.1 to 6.7mV. Featuring smaller clock tree skew and latency, the BS-only clock delivers a 4.7% speed gain over the FS clock. Combining above benefits, BS-only clock has 17.9% speed and 18.0% area benefits over FSPDN at the chip level.**

Keywords: BSI, BSPDN, BS clock, GAAFET, Nanosheet (NSH), Power Integrity (PI), Signal Integrity (SI).

Introduction: The continuous logic scaling demands the breakthroughs of architecture innovations [1], among which backside (BS) interconnect (BSI) and contact (BSC) emerge as the key enablers. Despite that GAA is generally accepted as the 2nm-class logic technology [1-3], its evolution beyond 2nm node calls for the co-optimization of contact (BS direct contact) and interconnect (BSPDN, BS Clock) by systematically evaluating their interactions. Meanwhile, the insertion points of these optimizations in the sub-2nm technology also urge multi-level analysis from processes, devices, circuits to systems.

To push the power-performance-area (PPA) frontier of Nanosheet (NSH) [4] FET, which are widely adopted in high-volume GAA production, this work studied two mainstream technologies in detail, namely BSPDN and BS clocking, to expand the potential of 2nm-class technology series for AI, high performance computing (HPC) and mobile SoC applications. By step-by-step incorporating these elements, a series of 2nm-class design rules (DRs) were adaptively transferred from FSPDN to BSI.

However, significant BS resources remain underutilized, upgrading from FSPDN to the full BSPDN. Thus, the BS clock, the initial phase of BS inter-cell [5-6] routing, manages leveraging wide BS metal for routing global clock nets to mitigate FS routing congestion mainly induced by the extreme-scaling standard cell (STC) height (<130 nm generally in sub-2nm nodes) and to construct more robust clock tree. Furthermore, in the presence of both BSPDN and BS global nets, the PI/SI trade-offs occur and were studied for the first time (Fig. 1). The chip-level PPA, clock quality, SI, and PI assessments from FSPDN to BS clock further validate solid benefits on the progression of BSI.

BSI Architecture Evolution on a 2nm-class Platform:

Extending from industry reports [1-3], based on NSH, BSI evolution accompanied by practical DRs was first proposed with the migration of all power and some signals from FS to BS (Fig. 2(a)). On one hand, the scaling of STC height towards 2nm-class nodes is facilitated not only by the shrinks of NS width (W_{NS}) and pitch, but also by the movement of VDD and GND nets to the BS combining with BS direct contact process. Consequently, targeting the 2nm-class DR, a subtle reduction in STC height (from 130 nm to 120 nm) and a relaxation of FS signal dimensions emerge on account of PDN relocation to the BS. On the other hand, as the transition from BSPDN to inter-cell routing, one signal line is inserted between the BS power rails to support the stronger BS clock network build-up at the same STC height. In the future, more BS signal lines is required to squeeze out the BS resource for dual-sided routing under the further shrinkage of STC height, along with the depopulation of FS signal tracks.

To establish a solid baseline for circuit– to chip-level evaluations, a series of stringent DTCO procedures were conducted. STC libraries with more than 40 basic cells were established on a 2nm GAA baseline (more design variants with dual-sided pins for implementing BS clock network) and characterized by well-calibrated SPICE/PEX decks (Fig. 2(b)) [2, 7]. Notably, all device and parasitic models, based on the calibrated 2nm silicon data [2] and targeted at the same V_t of 0.15 V, were used in the library characterization and RO assessment (Figs. 3(a-b)). To anchor circuit-level evaluation in the realistic chip operation, BEOL loads from critical paths (CPs) of a 32-bit RISC-V core [8] were extracted and applied to the 15-stage INVD1-based RO with fan-out 3 to evaluate the power-performance of various BSI architectures.

Regarding the process enablement, Fig. 4 shows dual-sided interconnects demonstrated on a FinFET test vehicle. In terms of BSI process integration options, this research focuses on the BSC approach [9], considering its better performance, superior BS utilization and clear cell height reduction over BPR [10] and PowerVia [11]. As process flow schematic drawn in Fig. 5, BS direct contact [12], eliminating the high-aspect-ratio and high-resistance contact via by placeholder (PH) [13], features more straightforward litho-defined direct BS contact plug to the wide source/drain (S/D) bottom of NSH.

For BS inter-cell routability [6], BSC is also the optimum, which naturally enables BS pin access [14] and achieves the lowest resistance. Therefore, BSC is the key to STC designs with balanced FS/BS pins and thus symmetric FS-BS routing, for which it is adopted throughout 2-nm class technologies with BSI evolutions. With progressive device and interconnect architecture advancements above, 2nm-class GAA series with BSPDN and BS clock + BSPDN obtain circuit-level speed gains of 15.3% and 26.9% over the one with FSPDN at iso-power, respectively (Fig. 6).

Chip-level PPA & SI-aware Analysis:

Fig. 7 outlines the chip-level evaluation framework used to assess PPA, PI, SI and clock quality on the 32-bit RISC-V cores [15]. It includes the physical implementation of BSPDN, BS clock tree synthesis and dual-sided routing (first report on GAA platform with 2nm design rules). Particularly, the trunk/leaf nets of the BS clock are entirely routed on the BS using STCs with both BS input and BS output pins (e.g., BS_BUF), whereas the BS clock sinks are registers that only require BS input pins (e.g., BS_DFQ). This clock architecture is referred to as a BS-only clock. (Fig. 8 (a)). At the same DR (120 nm STC height and 42 nm CGP), the 8.5% reduction in clock tree latency [16] and 9.3% reduction in skew (Fig. 8 (b-c)) clearly illustrate the superior quality of BS-only clock network, which outperforms the FS clock by 4.7% (Fig. 9(a)). Furthermore, the BS-only clock also contributes to relief the crosstalk on clock nets, which are typically part of the critical paths (CPs), by shielding clock nets from surrounding non-clock aggressor signals, thereby resulting in 25.9% smaller Δ CP delay than FS clock (Figs. 9(b)). At the chip-level, BS clock and BSPDN obtain progressive iso-power frequency boosts of 17.9%/10.3% over the starting FSPDN, with reductions of 20.8%/14.3 in EDP and maximum reduction of 47.3% in area (Figs. 9(c-d)).

PI-aware Assessment:

Dynamic voltage (IR) drop (DvD) analyses were also performed from FSPDN to BSPDN with BS clock. Pure BSPDN achieves optimal instance IR drop (i.e. the cumulative voltage drops across both VDD and VSS PDNs for each STC placed inside a chip) with 5.1 mV DvD, benefited from its tight power mesh and relaxed metal dimensions (TABLE II). However, the DvD rises to 6.7 mV when BS clock shares the BS metal resource (Fig. 10), respectively. This increase is well expected considering the reduction in power mesh density from more signal nets routed on the BS for the shift from BSPDN to BS inter-cell routing, revealing the trade-off between PI and SI.

Conclusion: In this work, empowered by 3D device architecture and the evolution of dual-sided interconnects, a couple of backside interconnect innovations were studied on 2nm GAA technology series. Considering the more challenging signal and power trade-off issues with BS global nets, SI and PI were examined systematically at the chip level for the first time. Pure BSPDN achieves the best PI through a tight BS power mesh, and BS clock delivers optimal clock quality with BS-only clock tree. From the PPA, SI, clock timing and PI analysis, GAA technology with BSI advancements, regarded as the last planar-integrated technology before stacked transistor, paves a sustainable path for AI, HPC, and mobile.

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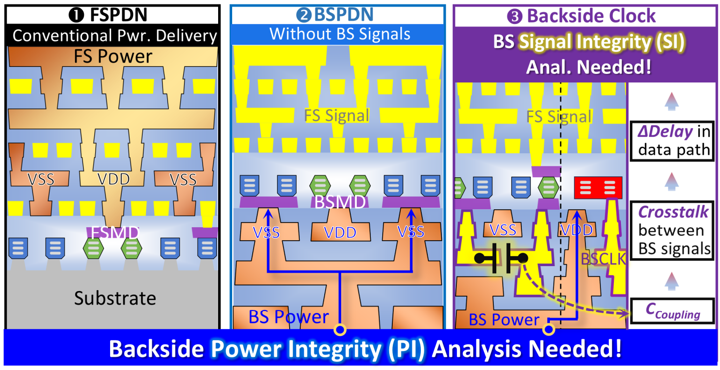


Fig. 1 Backside (BS) interconnect evolution. Frontside (FS) PDN advances to BSPDN and to BS clock. The BS power and signal require systematic power integrity (PI) and signal integrity (SI) analysis at the chip level.

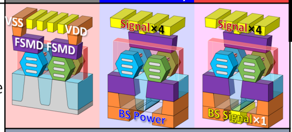
Tech.	FSPDN	BSPDN-only	BS Clock
Channel Structure			
	3-Stack Nanosheet (NS)		
Intc. Arch.	FS Routing	+ BS Power	+ BS Clock + BS Intra-cell Routing
CPP (nm)	48	45	42
L_g (nm)	16	14	12
W_{NS} (nm)	18	16	16
M0P(nm)	22	30	30
M2P(nm)	26	30	30
CH (nm)	130	120	120

Fig. 2 Progression of interconnect architecture from FSPDN, BSPDN to BS clock+BSPDN and related design rules.

TABLE I. Std. cell Libraries for chip-level evaluation

INVD1/2/4/8	NAND3D1
BUFD1/2/4/8	NAND4D1
NAND2D1	AND3D1
NAND2D2	AND4D1
AND2D1	NOR3D1
AND2D2	NOR4D1
NOR2D1	OR3D1
NOR2D2	OR4D1
OR2D1	OAI21D1
OR2D2	OAI22D1
XNR2D1	OAI31D1
AOI21D1	OAI211D1
AOI22D1	OAI311D1
AOI31D1	OAI222D1
AOI211D1	MUX2D1
AOI311D1	MUX2D2
DFQD1	DFQRSD1

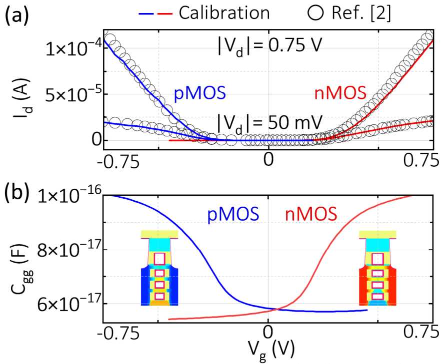


Fig. 3 (a) I_d-V_g transfer curves at |Vd| = 0.05/0.75 V calibrated to 2nm-class silicon data [2] and (b) C_{gg}-V_g curves calibrated by device structure.

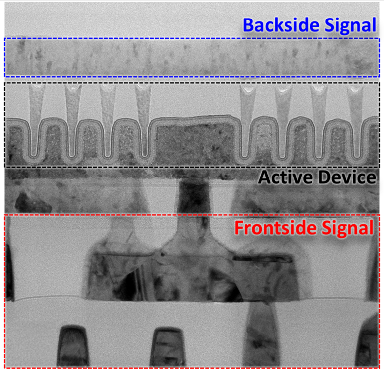


Fig. 4 TEM of BS interconnect verified on a FinFET test vehicle. Signal metal line was fabricated experimentally on the wafer BS.

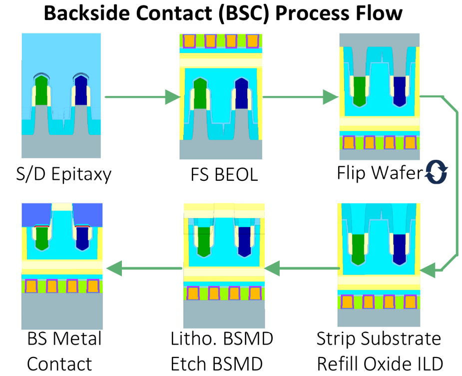


Fig. 5 Process flow schematic highlights the critical backside (BS) fabrication steps and treatments of BS direct contact (BSC).

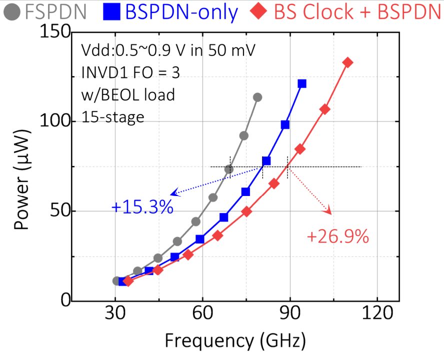


Fig. 6 RO PP benchmark across BSI architectures from FSPDN to BS clock with FO3 and BEOL load. BS clock shows the largest circuit-level speed gain, reaching 26.9% relative to FSPDN.

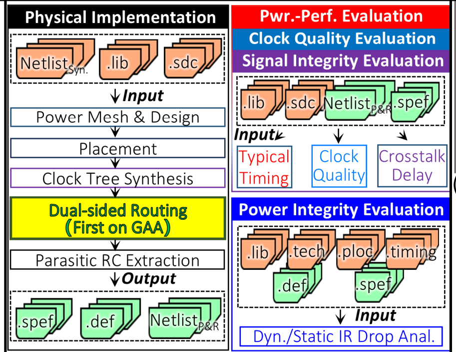


Fig. 7 Chip-level physical implementation & systematic evaluation framework with multi-dimensional analysis of pwr.-perf., signal integrity (SI), clock quality, and power integrity (PI).

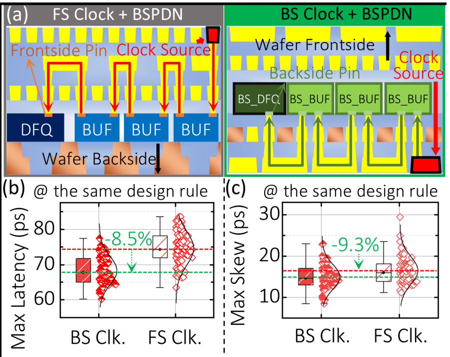


Fig. 8 (a) the comparison of FS and BS-only clk. path that requires BS_BUF. The BS-only clk. obtains reduction of (b) 8.5% maximum latency and (c) 9.3% maximum skew over the FS clock.

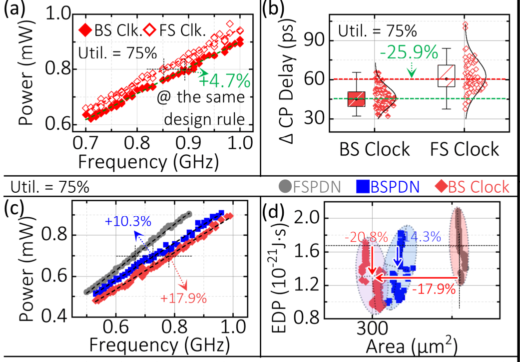


Fig. 9 Chip-level SI analysis & PPA results: (a) BS clock outperforms FS clock by 4.7% at the same design rule, also benefited from (b) ΔCP delay reduction of 25.9%. (c) Pwr.-perf. and (d) EDP-area readouts.

TABLE II. Power mesh designs & rules

FSPDN			BSPDN		
FM1	32 nm	Totem	BM1	42 nm	Grid
FM2	26 nm	Staple	BM2-3	76 nm	Grid
FM3	35 nm	Grid	BM4-5	126 nm	Grid
FM4	35 nm	Staple	BS clock + BSPDN		
FM5	42 nm	Staple	BM1	42 nm	Staple
FM6-8	76 nm	Staple	BM2	76 nm	Staple
FM9-11	76 nm	Grid	BM3	76 nm	Staple
FM12-13	126 nm	Grid	BM4-5	126 nm	Grid

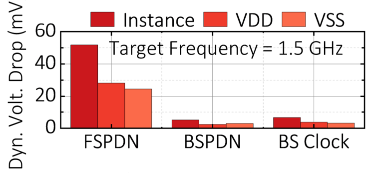


Fig. 10 PI analysis: Dyn. volt. drop (DvD) comparison. Pure BSPDN achieves the lowest DvD. Slight DvD bounce is observed when clock is allocated to the BS.

TABLE III. Benchmark with the previous research

	[2]Samsung VLSI24	[7]AMAT IEDM24	[11]Postech VLSI24	[14]GIT VLSI24	This Work
BSPDN IR Drop Analysis	×	×	√	√	√
Sig. Tranf. Cell /nTSV needed	Sig. Tranf. Cell	N/A	Opt.	nTSV	Opt.
BS Intra-Cell Routing	√	√	√	N/A	√
Standard Cell BS Pin	√	×	√	N/A	√
BS Clock Routing	√	N/A	×	√	√

References: [1] J. Jeong *et al.*, *VLSI*, 2023 [2] G. Yeap *et al.*, *IEDM*, 2024. [3] K. Fischer *et al.*, *VLSI*, 2025. [4] N. Loubet *et al.*, *VLSI*, 2017. [5] J. Lee *et al.*, *VLSI*, 2025. [6] A. Pal *et al.*, *IEDM*, 2024. [7] C. -H. Chang *et al.*, *VLSI*, 2025. [8] H. Wu *et al.*, *EDTM*, 2025. [9] B. Kim *et al.*, *VLSI*, 2024. [10] A. Veloso *et al.*, *IEDM*, 2023. [11] M. Shamanna *et al.*, *VLSI*, 2023. [12] S. Liao *et al.*, *IEDM*, 2024. [13] R. Xie *et al.*, *VLSI*, 2024. [14] J. Ahn *et al.*, *DAC*, 2025. [15] H. Lu *et al.*, *DATE*, 2025. [16] P. Vanna-iampikul *et al.*, *VLSI*, 2024.